## **REMARKS**

Claims 1-11 are pending in this application. By this Amendment, claims 1, 2 and 5-8 are amended. Claims 9-11 are added. No new matter is added.

#### I. Objections to the Specification

The specification is objected to for allegedly introducing new matter into the disclosure of the invention by way of the Preliminary Amendment filed on July 7, 2003. The specification is amended in response to the objection.

Although the Abstract has not been objected to, the Abstract is amended to remove legal phraseology and reduce the length of the Abstract to less than 150 words in accordance with 37 C.F.R. §1.72.

# II. Claim Rejections Under 35 U.S.C. §112

Claims 1-8 are rejected under 35 U.S.C. §112, second paragraph. Specifically, the Office Action states that claims 1 and 2 recite that the recited feature "the surface" in lines 10 and 11 of claims 1 and 2, respectively is unclear. Claims 1 and 2 are amended in response to the rejection. Accordingly, Applicants respectfully request the rejection of claims 1-8 under 35 U.S.C. §112, second paragraph, be withdrawn.

## III. Claim Rejections Under 35 U.S.C. §103

Claims 1-8 are rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 6,309,971 to Geha, in view of U.S. Patent No. 6,002,175 to Maekawa, and further in view of U.S. Patent No. 6,077,782 to Hsu et al. (Hsu). The rejection is respectfully traversed.

Applicants assert that none of the applied references, whether considered alone or in combination, disclose or suggest each and every feature recited in the rejected claims. For example, the combination of references does not disclose or suggest a method of fabricating a semiconductor device . . . comprising . . . forming a via-hole in an interlayer dielectric formed above the first wiring region on a semiconductor substrate; removing gaseous components

included within the interlayer dielectric by a heat treatment under reduced pressure and at a substrate temperature of 300°C to 500°C; forming a wetting layer on a surface of the interlayer dielectric; forming a first aluminum layer comprising one of aluminum and an alloy in which aluminum is the main component on the wetting layer at a temperature at a first degree C; forming a second aluminum layer comprising one of aluminum and an alloy in which aluminum is the main component on the first aluminum layer at a temperature of a second degree C; and the first degree C is lower than the second degree C.

The Office Action alleges that Geha teaches all of the steps recited in the rejected claims but fails to explicitly teach forming a wetting layer on the dielectric and a degassing step via a heat treatment under reduced pressure at the substrate temperature of 300°C to 550 °C.

Geha relates to metallization processes for use in making devices such as semiconductor devices. Geha discloses a cold deposition step 201, in which a first amount of metal 804 is deposited on a substrate surface 801. When the substrate is a semiconductor wafer, the first amount of metal is deposited shortly after the wafer has been processed in some other manner, such as deposition of a wetting layer of titanium or titanium-tungsten, that causes the temperature of the wafer to be elevated. The temperature of the wafer during step 201 can be from about 40°C to about 250°C and preferably about 200°C (col. 6, lines 12-26 and Fig. 8).

To overcome the admitted deficiencies, the Office Action first combines Maekawa and alleges that Maekawa teaches a degassing step for removing gaseous components included within an interlayer dielectric by a heat treatment under reduced pressure and at the substrate temperature of 300°C to 550°C.

Maekawa relates to the structure of a connection hole in which a second electrically conductive layer is embedded for electrically connecting a first conductive layer to a second

conductive layer with an insulating layer formed between the two layers. Maekawa addresses the problem of the connection hole being blocked by deposition of the second conductive layer by sputtering (col. 1, lines 25-63, Figs. 35-38).

In Maekawa, a connection hole 4 is formed through the insulating layer 3 by a photoengraving process (see Fig. 4, col. 6, lines 64-67). After the connection hole is formed, water, nitrogen, hydrogen or an organic substance clinging to the surface of the semiconductor device is removed by degassing in which the substances are removed by heating to a temperature of 150 to 600°C in a high vacuum of inner gas such as argon (col. 7, lines 1-9). A barrier layer 5 is then formed on the first electrically conductive layer 2 (see Fig. 5). The barrier layer is formed by depositing TiN onto the insulation layer 3. A second electrically conductive layer 6 consisting of an aluminum alloy is then deposited on the insulating layer 3 and inside the connection hole 4 in a vacuum. Deposition of the second layer results in a gap 7 between the second electrically conductive layer 6 over the connection hole 4, partially blocking the hole. As a second electrically conductive layer 6 is further deposited, a space 8 is left inside the connection hole 4, as shown in Fig. 7 (col. 7, lines 19-55). The space 8 is removed by keeping the second electrically conductive layer 6 under high temperature and pressure in the vacuum continuity, the second electrically conductive layer is kept under the temperature of 300 to 600°C and a pressure of 200 to 900 km per cm<sup>2</sup> in an atmosphere of inert gas such as argon.

Thus, in Maekawa, the method includes depositing a first electrically conductive layer on a semiconductor substrate forming the insulating layer, forming the connection hole, degassing the semiconductor device, forming the barrier layer, and then depositing the second electrically conductive layer in such a way as to remove the gap or space formed in the connection hole 4 by the second conductive layer 6. Although Maekawa discloses a degassing, as alleged in the Office Action, degassing (removing gaseous components) is not

performed as recited in the rejected claims. For example, degassing in Maekawa is done after the first conductive layer is deposited and before the second conductive layer is deposited. In contrast, removal of the gaseous components in the rejected claims is performed prior to either of forming the first aluminum layer on the wetting layer or forming the second aluminum layer on the first aluminum layer. Thus, Maekawa does not contemplate the process as recited in the claims.

Furthermore, in Maekawa, the second electrically conductive layer is deposited over the barrier layer. In contrast, in the rejected claims, the second metal layer is formed on the first metal layer.

The Office Action further alleges that Hsu teaches forming a wetting layer on a dielectric. Hsu relates to integrated circuit structures and fabrication methods. Specifically, Hsu discloses a method to reduce electromigration by controlling the deposition conditions and textures of the substrates. For example, it is known that the formation of aluminum alloy thin films with certain crystalline orientations (texture) enhances the electromigration resistance. To reduce such electromigration, liners are commonly used such as titanium and TiN. Hsu addresses improving the texture of titanium and aluminum which will reduce electromigration by controlling deposition conditions on substrates (col. 1, line 45 - col. 2, line 28). Although Hsu discloses wetting, i.e., Ti/TiN deposition at Fig. 2C, Hsu does not disclose or suggest forming a second layer comprising one of aluminum and an aluminum alloy on the first aluminum layer, as recited in the claims.

Furthermore, none of the applied references whether considered alone or in combination disclose cooling the substrate to a temperature of no more than 100°C formed after the step of forming a wetting layer on a surface of the interlayer dielectric. For example, Geha fails to disclose the relationship of the temperature control between forming a wetting

layer and forming a first aluminum layer. Furthermore, neither Maekawa or Hsu disclose or suggest such a relationship.

In contrast, by employing the steps of cooling the substrate to a temperature of no more than 100°C after the step of forming a wetting layer, the advantage of accurately adjusting the temperature and the advantage of minimizing the amount of gas that escapes from an interlayer dielectric, a wetting layer and a wafer during the formation of the first layer are achieved. For example, the cooling of the substrate temperature ensures that the substrate temperature is lower sufficiently prior to forming the first aluminum layer. Because the previous degassing step is performed at a high substrate temperature exceeding 300°C, lowering the substrate temperature ensures that the temperature can be adjusted reliably for the subsequent step. Thus, the cooling steps enable the process to minimize the amount of gases emitted from the interlayer dielectric, wetting layer, and also the entire surface of a wafer during the formation of the first aluminum layer. As a result, the adsorbtion at the interface between the wetting layer and the first aluminum layer, from adversely affected the coverage performance adhesiveness, is prevented.

Thus, none of the applied references of record whether considered alone or in combination disclose or suggest forming a second aluminum layer on a first aluminum layer using the method as recited in the rejected claims. Accordingly, Applicants respectfully request the rejection of claims 1-8 under 35 U.S.C. §103(a) be withdrawn.

### III. <u>Double Patenting</u>

Claims 1-8 are also rejected under the Judicially Created Doctrine of Obviousness-Type Double Patenting as being unpatentable over claims 1-5 of U.S. Patent No. 6,107,182 to Asahina et al. The Office Action states that "although the conflicting claims are not identical, they are not patentably distinct from each other because the species claimed in the conflicting

Application No. 10/613,065

patent anticipates the claims genus of the present application". The rejection is respectfully

traversed.

Applicants submit that a Terminal Disclaimer in compliance with 37 C.F.R. §1.321(b)

and (c) is filed concurrently herein (copy enclosed). Accordingly, Applicants respectfully

request the rejection be withdrawn.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in

condition for allowance. Favorable reconsideration and prompt allowance of claims 1-11 are

earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place

this application in even better condition for allowance, the Examiner is invited to contact the

undersigned at the telephone number set forth below.

Respectfully submitted

James A. Oliff

Registration No. 27,075

John W. Fitzpatrick

Registration No. 41,018

JAO:JWF/ldg

Attachment:

Terminal Disclaimer

Date: September 29, 2004

OLIFF & BERRIDGE, PLC

P.O. Box 19928

Alexandria, Virginia 22320

Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE **AUTHORIZATION** 

Please grant any extension necessary for entry; Charge any fee due to our

Deposit Account No. 15-0461